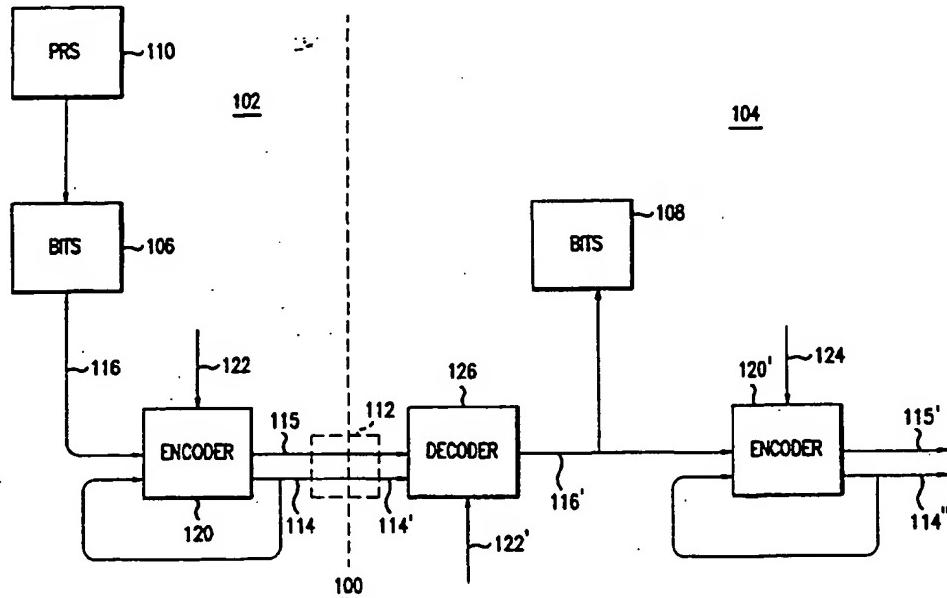




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H04J 3/06	A1	(11) International Publication Number: WO 96/39761 (43) International Publication Date: 12 December 1996 (12.12.96)
(21) International Application Number: PCT/US96/07909		(81) Designated States: CA, JP, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).
(22) International Filing Date: 29 May 1996 (29.05.96)		
(30) Priority Data: 08/471,410 6 June 1995 (06.06.95) US		Published <i>With international search report.</i>
(71) Applicant: SYMMETRICOM, INC. [US/US]; 85 West Tasman Drive, San Jose, CA 95134-1703 (US).		
(72) Inventors: NARASIMHA, Midihally; 14099 Elvira Street, Saratoga, CA 95070 (US). SHENOI, Kishan; 20655 Verde Vista Lane, Saratoga, CA 95070 (US).		
(74) Agents: SIMON, David, M. et al.; Loeb & Loeb L.L.P., Suite 2200, 10100 Santa Monica Boulevard, Los Angeles, CA 90067 (US).		

(54) Title: ENCODING SYSTEM FOR DISTRIBUTION OF SYNCHRONIZATION



(57) Abstract

Apparatus and methods for distributing synchronization throughout a network is disclosed. The distribution of the synchronization is through the use of generating a reference timing signal, and by counting the line clock pulses between the start of a frame and the timing reference signal pulse at a first office and that count is then encoded and transmitted to the next office. At the next office, the transmitted count is decoded and used for regenerating synchronization by counting a number of received line clock pulses from the start of the frame to regenerate the reference timing signal. Particular criteria for selecting the frequencies for the timing reference signal are disclosed.

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ENCODING SYSTEM FOR
DISTRIBUTION OF SYNCHRONIZATION

Background of the Invention

5 Field of the Invention

This invention relates to providing synchronization distribution throughout a network and in particular relates to providing this distribution in a synchronous optical communications environment prevalent in telephone networks.

10

Description of the Environment

In digital telephone networks, the network is comprised of hundreds or even thousands of offices or nodes such as shown in simplified form in Figure 1. The network 10 has a plurality of offices 12, 14, 16, 18, 20. Each node has a local timing source 12a, 14a, 16a, 18a, 20a, commonly called a BITS for Building Integrated Timing Supply. Also, each node has a variety of equipment such as switches, optical multiplexers, channel blanks, etc. 20 commonly referred to as network elements (NE's) 12b, 14b,

16b, 18b, 20b, with the timing for each network element within the office being supplied by the office's BITS. The various offices within the network are connected by copper or optical fiber links 22 called facilities. Unlike the earlier versions of the copper based networks where the facilities formed a mesh type network with each office being linked to multiple offices by several facilities, digital optical networks are arranged in chains or rings with facilities tying each office typically to the two adjacent offices.

Further, in a typical digital network, there are a plurality of primary reference source checks called PRS checks. Typically, the PRS clocks are implemented using cesium beam or GPS receiver technology. The PRS clocks serve as master clocks and provide a timing reference for the remainder of the network. The PRS timing is communicated over the facilities to different nodes to permit synchronization between various nodes within the network.

The earlier (non-standard versions of the optical fiber network employed asynchronous bit stuffing techniques to multiplex the input tributary signals onto the optical line. The distribution of the timing reference in such a

network may be realized using a embedded DS1 signal, as shown in Figure 2. The PRS timing 30 in an office 32 is provided to the BITS 35 and then to fiber multiplexer 36 in a first office and communicated to the next office 40 over the embedded DS1 signal in the optical facility 38. Further, the fiber multiplexer 42 at the next office 40 recovers the DS1 clock 44 and passes that recovered clock to the BITS 46 of the second office and to the fiber multiplexer 48 for transmission over the next facility in the chain to the next office. Since the BITS clock 46 is not used for generating the line timing signal 50 provided to the next office in the chain (not shown), inaccuracies in the timing reference communicated to the BITS timing in intervening offices do not effect the timing reference communicated to the BITS of the successive offices. Thus, if the BITS timing reference in the second office malfunctions, the synchronization of the successive nodes or offices (not shown) in the network is unaffected. Therefore, each of the nodes or offices in the network may be thought of receiving its synchronization timing directly from the offices containing the PRS. Where each of the nodes of the network is receiving the timing reference directly from the PRS, synchronization may be thought of as

being at the same level. Such distribution schemes of synchronization are referred to as being flat.

Although the method described above yields the desirable flat synchronization distribution system, it is not deployed extensively in the telephone network for two reasons. First, the bit stuffing operation performed at each node adds jitter to the embedded DS1 synchronization reference. This may render the DS1 signal unusable as a timing reference after it traverses a few nodes. Second, and more important, the nonstandard asynchronous optical fiber systems are being replaced by the recently developed standard synchronous optical network technologies, designated as SONET or SDH. The method of distributing the synchronization reference using an embedded DS1 signal does not work properly in the SONET environment, as explained below.

In a SONET multiplexer, the output optical line clock is normally synchronized to the office BITS clock. The rate variations between the input tributaries and the output line signal are accommodated by a byte stuffing process known as pointer adjustment. The eight bit phase movements caused by the pointer adjustments can be large enough to render the embedded DS1 timing reference incapable of

adequately transporting the synchronization information.

Hence, the standards organizations (ANSI and the ITU) recommend that a DS1 signal embedded within a SONET line signal not be used for synchronization distribution.

5 Instead they recommend the use of the recovered optical line clock to generate a derived DS1 synchronization signal. This derived DS1 signal serves as the synchronization reference input to the office BITS clock.

10 The use of the derived DS1 to distribute synchronization references, however, implies a hierarchical synchronization network. In such a network, the BITS clock at an intermediate node is not synchronized directly to the PRS but is instead synchronized to the timing reference supplied by the BITS clock in the previous node. This
15 hierarchical scheme for the distribution of synchronization signals has many shortcomings.

First, administrative controls are required to ensure that a higher quality BITS clock (lower stratum number) does not accept timing from a lower quality BITS clock.
20 Second, the cascade of clocks created by the hierarchical chain can impair the timing reference traversing the network. Third, if a BITS clock fails anywhere in the chain, all the downstream clocks will lose

synchronization. And finally, this scheme is prone to the inadvertent creation of timing loops, especially under facility failure conditions. (A timing loop occurs when timing from a first node is passed to the second node and then the timing is fed back through a chain of one or more additional nodes to the first node so that the first node is synchronizing its timing to itself. Such a situation is clearly undesirable since all the nodes involved in the timing loop will be isolated from the PRS).

10 Synchronization messaging is a solution recommended by the standards organizations to alleviate some of the shortcomings delineated above. In this method, the status of the clock that generates the timing reference at a particular node is communicated to the clocks and network elements at other nodes over a messaging channel. The clocks at these other nodes will then decide, in an intelligent manner, whether they should synchronize to one of the incoming timing references, or whether they should operate in a holdover mode. However, the synchronization messaging scheme does not cure all the problems created by the hierarchical synchronization distribution network. Furthermore, implementation of this messaging scheme will be expensive as it involves the retrofitting of the

existing BITS clocks and the SONET network elements to provide this capability.

Therefore, it is the first objective of this invention to provide a method for transporting network synchronization reference signals over the existing SONET network using a flat distribution scheme. It is a second objective of this invention to distribute these synchronization reference signals without incurring the problems associated with the hierarchical scheme. It is yet 10 a third objective of this invention to achieve the flat synchronization distribution system without requiring substantial hardware investment or retrofitting costs.

Summary of the Invention

These and other objects are achieved by relying on two timing elements available at each office: the line clock and the SONET frame timing. A timing reference signal synchronized to the PRS and at a frequency that is at least slightly less than the frame rate is generated at the originating PRS site. The line clock is then used to determine the interval between the start of the frame and an edge of the timing reference signal. This timing difference is encoded and transmitted in an overhead channel and may be decoded at the next node. The next node may then recover the timing reference for use in its own BITS timing and for transmission on to the next node.

Therefore, a flat synchronization structure is created as each node in the network depends for its timing upon the original PRS instead of the intervening nodes. Further, this flat structure eliminates any possibility of timing loops.

To fit this approach in existing network structures without substantial hardware costs, a few counters, flip-flops, and gates can be used to generate all of the timing signals. To reduce messaging overhead, the encoded timing difference can be transmitted over multiple frames in

currently used control bytes reserved in the SONET architecture.

Description of the Drawings

5 FIGURE 1 is a diagram of a simple prior art telephone network.

FIGURE 2 is a diagram of the synchronization distribution scheme in a prior art asynchronous network.

10 FIGURE 3 is a block diagram for an encoder and a decoder for an embodiment of the invention.

FIGURES 4A and 4B are timing diagrams relating to the embodiment of FIGURE 3.

FIGURE 5 is a functional flow diagram for the embodiment of FIGURE 3.

15 FIGURES 6A and 6b are schematics of circuits for retiming the timing reference signal at the encoder.

FIGURE 7A is a schematic of a circuit in the encoder for measuring the timing difference between the start of the frame and the timing reference signal.

20 FIGURE 7B is the timing diagram for FIGURE 7A.

FIGURE 8 is a schematic of a circuit in the encoder for generating a flag to indicate in which frame an edge of the timing reference signal has occurred.

FIGURE 9A shows a circuit in the encoder for sampling the measured timing difference and the flag.

FIGURE 9B is the timing diagram for FIGURE 9A.

FIGURE 10A is a circuit in the decoder for generating the timing reference signal in the decoder.

FIGURE 10B is the timing diagram for FIGURE 10A.

FIGURE 11 is a circuit for generating a substitute for the timing reference signal when certain error conditions are detected.

10

Detailed Description of the Invention

The embodiments of the invention involve transmission of synchronization of timing. FIGURE 3 is useful in explaining an embodiment of the invention, as applied in a SONET or similar synchronous optical environment. A portion 100 of the network is shown in FIGURE 3. Each node or office 102, 104, in the network has a BITS clock source 106, 108 and at least one node has a PRS 110 directly controlling the BITS timing 106. Each node receives and transmits a line clock LCLK 114 over a facility such as an optical fiber 112 linking nodes. Each node also receives and transmits frames at a nominal rate of eight thousand times a second with the frame containing control

information and data according to the established network protocol. In the SONET environment, the duration of a frame is nominally one hundred twenty five microseconds.

A locally generated timing reference signal 116 generated

5 from the BITS timing signal (the BITS timing signal is nominally a 1.544 MHz signal in SONET) is also provided in each node having a PRS. Also generated internally by the office or node 102 is a frame start signal LFRM 122. The frame start signal and the line clock can be obtained from
10 the add-drop multiplexer (ADM, not shown) at the office.

An encoder 120 measures the difference in timing between the start of the frame as indicated by the frame start signal, signal LFRM 122 and the timing reference signal 116. This timing difference may be obtained by

15 counting the line clock pulses between the start of the frame as indicated by LFRM and a pulse edge of the locally generated timing reference signal. The timing difference represented by this count may be encoded into reserved control bytes of the message frame 115 and may then be

20 transmitted over the facility 112 to the next office 104 in the SONET chain or ring. At this second office, a decoder 126 uses the transmitted line clock 114' that has been transmitted from the office 102 and recovered in the office

104 by the ADM (not shown) along with a line frame start signal 122' that has been reconstructed by the office ADM according to well known techniques in the art. In a manner explained below, the local timing reference signal 116' can be regenerated, for example, by multiplying the period of the line clock LCLK 114 by the transmitted count 115 to generate a pulse in a manner that will be described in more detail below.

5 That regenerated timing signal 116' may then be supplied to a further encoder 120' that also receives the start of the frame signal 124 generated by the office for the frames to be transmitted. The line clock 114'' for transmission to the next node in the chain of the network (not shown) is also provided to the encoder 120' from the 10 ADM (not shown). The difference between the start of the frame pulse LFRM 124 and the regenerated timing signal 116' may be counted with the line clock to provide a further count 115' for transmission over the facility (not shown).

15 FIGURE 4A shows a timing chart relevant to time measurement at the first office 102. The 51.84 MHz line clock LCLK 114 provides the fundamental reference for counting periods or bit times for the time measurement.

The start of each successive frames N-1, N, N+1, N+2 is indicated by the rising edge of a pulse in the frame start signal LFRM 122. Since a frame has a duration of 125 microseconds, there are 6480 possible periods of the line clock LCLK in which an edge of the timing reference signal 116 can occur. In the instance in frame N, the edge occurs during the fourth bit time measured in units of the 51.84 MHz clock so a count of four would be encoded. During the next frame (N+1) or some subsequent frame, that count may be transmitted to the next node 104 over the link 112.

Upon receipt of the count, the next node 104 in the network will generate a rising edge of a reconstructed timing reference signal 116' at the start of the fourth received bit time in the N+K frame as shown in FIGURE 4B. In particular, the decoder 126 will receive the regenerated line clock LCLK 114' generated by the ADM at the office 104 and count a number of cycles of that clock equal to the received count. At that point, the decoder will generate an edge in a regenerated timing reference signal 116' that may be used in the office 104 for synchronizing the BITS 108 to the PRS 102. In addition, the line clock, the regenerated timing signal 116' and the local frame start signal 124 from the second office's 104 SONET ADM (not

shown) may be used for measuring the difference and transmitting a count to the next office so that it may also generate a local version of the timing signal. Since each version of the timing signal is only dependent upon the PRS timing and not the BITS timing of each local office in the chain, distribution of the timing tied to the timing reference is flat and avoids both timing loops and hierarchy problems.

Figure 5 shows a functional flow diagram of distribution of timing throughout the network. Successive offices N-1, N and N+1 in a network perform the function of measuring the timing difference between a timing reference signal and the line clock and the start of the frame using the transmit line clock. The measured time difference at node N-1 is encoded and then transmitted over a link 150. At the next node, or office N, the line clock and the frame timing are recovered, the transmitted count is decoded and used to regenerate the timing reference signal. This regenerated timing reference signal is supplied to the BITS at office N for synchronization. This regenerated timing reference signal at office N is also supplied for measuring the timing difference with the start of the frame at office N to be transmitted to the next node using the transmit

line clock and frame timing of office N. The timing difference measured at office N is encoded and transmitted over the facility for subsequent recovery, decoding and regeneration at office N+1 in a like manner.

5 Selection of the appropriate criteria for the local timing reference signal is based upon several factors. First, the local timing signal pulse edge should occur no more than once each frame. Therefore, the local timing signal should have a rate of less than or equal to the frequency of a frame; e.g., 8 KHz in a SONET network.

10 However, since the frame rate may be at a slightly lower rate and still be within the SONET specification, the local timing reference signal should preferably occur at a rate that is less than the minimum permitted frequency of the frames. Further, the frame rate and the timing signal rate should not be harmonics of each other. Optimally, they should be "as prime as possible" with respect to the measurement rate of the line clock, which is 51.84 MHz. In particular, the highest common factor of the frame rate of

15 8 KHz and the timing reference signal should be as low as possible to prevent the development of beats occurring with such sampling with the line clock. In addition, the timing rate signal should preferably be at a frequency readily

20

obtainable from frequencies in the office such as the BITS signal. For this reason, a timing rate of 7.72 KHz or an integral submultiple thereof (i.e., 3.86 KHz, 1.93 KHz, .965 KHz) are among the preferred frequencies for a SONET network. These frequencies can be readily generated from the 1.544 MHz BITS timing signal available in each office since 7.72 KHz is obtained readily by dividing the BITS signal by two hundred. In fact, for reasons discussed later, 1.93 KHz may preferably be used for optimal encoding in an overhead byte for transmission over a SONET network.

A further advantage of the 7.72 KHz timing signal or some integral submultiple thereof is avoidance of metastable states resulting from the synchronous nature of the various signals and the switching speed of the digital logic involved. In particular, with the line clock of 51.84 MHz, there is a window around each edge of the line clock in which the occurrence of an edge of the timing signal may not be detected due to the transistor switching delays inherent in the digital logic. Such metastable conditions would result in a delay in detecting the edge and hence inject a one clock period pulse offset in detecting the count representing the occurrence of the timing edge. If a signal having the same frequency as the

frame rate, or harmonic thereof, is selected, this metastable condition can persist over a substantial period of time. With the selection of 7.72 KHz or an integer submultiple of that frequency, any metastable events will be one time events that can readily be eliminated at the next office through the use of a phase lock loop in the generation of the timing reference signal. By use of 7.72 KHz or integer submultiples of 7.72 KHz, the edge to edge change in the timing reference signal ensures that if a timing signal edge occurs in the metastable region of the edge in the line clock for the logic, the next occurrence of the timing reference signal edge will not be during the metastable region.

FIGURES 6A through 11 show various circuitry and associated timing diagrams for generating and regenerating the timing reference signal at the various nodes throughout the network. It is assumed that in each of these circuits, the circuit components are synchronous. First, the timing signal REF should preferably be retimed to the timing of the line clock LCLK. FIGURE 6A shows a circuit for generating such retiming while reducing the likelihood of a metastable condition. The circuit comprises three edge triggered D flip-flops and the retimed timing signal output

is REFRT and its complement, REFRT_L. FIGURE 6B shows an alternative version of such a circuit.

FIGURE 7A shows a circuit for generating the count representing the timing difference in units of the line clock LCLK period between the pulse indicating the start of the frame N in signal LFRM, and the retimed timing reference signal. The rising edge of the start of the frame signal LFRM resets a thirteen bit counter 160 that counts the line clock LCLK. When the falling edge of the complementary retimed timing signal pulse RFRT_L occurs, it enables the input of a thirteen bit register 162 that is coupled to the output BIT TIME COUNT of the synch counter 160 and the line clock LCLK. The current value from the counter is clocked at this point into the shift register. The contents of this register, labelled COARSE OFFSET, represent the timing delay between the LFRM frame pulse and the retimed timing signal in units of time defined by the LCLK period. The contents of the counter are held in the register until the next edge of the retimed timing signal. FIGURE 7B depicts the associated timing diagram.

Since the retimed timing reference signal may not have an edge in each frame, a flag indicating when an edge has occurred is needed. FIGURE 8 shows a circuit that is

useful for generating the flag signal to indicate that an edge in RFRT_L occurred during the current frame. The circuit 170 receives the line clock LCLK, the retimed timing reference signal REFRT, the start of the frame signal LFRM, and a start of the frame signal delayed by one line clock period LFRMD1. Optionally, two inverters 172a and 172b may be provided between D flip flops 174 and 176 that generate a flag signal FLAG indicating an edge of the timing reference signal has occurred with a true value indicating a flag has occurred.

For subsequent transmission to the next node, the stored count must be sampled for encoding and transmitting. The flag and the coarse offset value are then stored as a fourteen bit word as shown in FIGURE 9A. The frame start timing signal LFRM is delayed by the line clock LCLK in a flip flop 182 to provide the LFRMD1 signal and that LFRMD1 signal enables a D flip-flop 184 and a register 186 circuit that receive as their inputs the FLAG and COARSE_OFFSET values. These two values are gated with the line clock LCLK for processing during the subsequent frame to provide the sampled fourteen bit entity FLAG_OFFSET. The FLAG_OFFSET comprises SAMPLED_FLAG and SAMPLED_COARSE_OFFSET. As shown in the timing diagram

Figure 9B, the FLAG_OFFSET value lags one frame behind where the edge of the retimed timing reference signal RFRT occurs (assuming an edge occurred during the prior frame).

If the resultant sampled coarse offset value has the
5 sampled flag high, that count value may then be processed by the office network element, such as an ADM, for transmission over the network to another node on the network according to the network protocol. For example, using the current SONET protocol, the network has a
10 overhead byte called the F1 byte that is unused and reserved for future applications. Therefore, it is possible to use the F1 byte for transmitting the synchronization information.

Given that the synchronization count (COARSE_OFFSET)
15 uses the SONET standard of an 8 KHz frame rate and a line clock of 51.84 MHz, the coarse offset requires thirteen bits to transmit the maximum possible count of 6479. Therefore, at a minimum, two F1 bytes in two separate frames may be used for transmitting the information.

20 However, for coding accuracy, it is more desirable to transmit the information over four frames and therefore use four F1 bytes to permit error detection. Therefore, to match this transmission rate of four frames, the frequency

of the timing reference signal should be 1.93 KHz or some integral submultiple of that rate. The timing edge that occurs in Frame N, is actually encoded and transmitted in a four frame sequence over the next four frames, N+1, N+2, N+3, and N+4. Regeneration of the edge at the receiving node when using this algorithm will occur at a minimum of five frames after the edge occurred at the transmitting node.

A possible format for the F1 bytes is shown in table 10 I below:

Byte No.	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
0	0	Edge ₁	Edge ₂	Coarse Offset 5 LSB				
1	0	Edge ₁	Edge ₂	Coarse Offset Next 5 Bits				
2	0	Edge ₁	Edge ₂	Coarse Offset 3 MSB	X	X		
3	1	X	X	CRC	CRC	CRC	CRC	CRC

According to this format, the most significant bit in each of the first three F1 bytes is set to a logical zero and the most significant bit for the last byte is set to 1 so that the last byte of a four frame sequence can be readily detected. Alternatively, the MSB of the first byte may be set as one to mark the start of a sequence and the three remaining bytes may be set to zero. Further, the 25 fifth and sixth bits in the first three F1 bytes of a four

frame sequence are called edge data and are used for determining during which frame of the prior four frame sequence an edge of the retimed timing reference signal occurred.

5 In this implementation, the receiving node office compares the edge data in each of the first three F1 bytes of a four frame sequence. Either a majority rules or a requirement of all three edge bit patterns being the same may be used to determine in which frame the edge occurred.

10 Transmitting different values for each of Edge₁ and Edge₂ for each of the first three frames for the four frame sequence can be used to indicate that no edge occurs during the four frame sequence, a link has been broken so synchronization to the PRS has been lost or a phase slippage greater than the predicted amount has occurred.

15 In addition, various such error conditions can be passed between the nodes by encoding such error conditions in the bits labelled with X.

20 The value of the coarse offset is encoded into the first three F1 bytes of the four frame sequence. Also, a cyclic redundancy check (CRC) sequence, or some other error detection mechanism, is transmitted in the F1 byte of the fourth frame for detecting transmission errors in the

transmitted Coarse Offset.

The bits labelled with X may be used for a variety of optional functions. For example, such bits may be used with the bits indicated as CRC for transmitting a nine bit error correction code instead of a CRC. A predetermined bit pattern for these bits may also indicate a phase slippage at the transmitting node that is greater than a predetermined threshold or the like to prevent propagation of phase errors. Detection of such errors is readily possible by either the transmitting or receiving office. In response to such conditions, the receiving office may disregard the transmitted count for a four byte sequence.

For example, the receiving office may compute an expected range of values for the received coarse offset based upon the relative frequency of the frame and the timing reference signal. The receiving office may disregard the received coarse offset if the value is beyond the expected range.

At the receiving node where the timing difference information (the encoded coarse offset count) is received, the timing difference information can be used to regenerate a timing reference signal with the use of the circuit 200 shown in FIGURE 10A. In particular, the regenerated

received and recovered line clock RLCLK and the regenerated received frame signal RLFRM are provided from the receiving office ADM (not shown). The transmitted F1 bytes are decoded by the receiving office in the chain to provide a reconstructed version of FLAG_OFFSET. This regenerated flag signal can be based upon the edge bits in each of the first three F1 bytes in the transmitted four frame sequence. Either a majority rules protocol or a requirement of all three sets of edge bit patterns matching can be used for determining in which frame the edge occurred. To match the flag signal at the equality detector, a logical "1" is also provided so that the pulse will be generated during the appropriate frame. The coarse offset can be obtained by concatenating the three portions of the coarse offset transmitted in the four-frame sequence.

The decoded FLAG_OFFSET is clocked into a register 202 that is enabled by the reconstructed start frame signal. Simultaneously, a thirteen bit counter 204 is counting the regenerated line clock RLCLK. Both the output of the counter 200 and the register 202 are provided to an equality detector 206. The equality detector can then provide a pulse when the count contents and the "one" to

match the flag and the contents of the register are equal.

The pulse from the output of the equality detector can then be provided to a D flip flop 208 to provide the regenerated timing reference signal REFREGEN. This regenerated timing signal is provided at least two frames plus one regenerated line clock period after the timing edge occurred. If the format described above using four frames for transmission of the timing difference is used, the delay will be at least five frames plus the one regenerated line clock period. Any other delays inherent in communications between the two offices may increase that delay. Nonetheless, such a regenerated reference timing signal does permit transmission of synchronization throughout a network in the manner described for FIGURES 3-5 above.

Further, although the use of the line clock at 51.84 MHZ provides a granularity of about twenty nanoseconds (the period of the line clock) with which to measure synchronization, this granularity can be reduced. To reduce the granularity, one may provide the recovered timing reference signal REFREGEN to a digital phase lock loop with a very narrow bandwidth, for example about one hertz. The granularity of the sampling of the frequency

with the line clock results in a poisson like distribution of error in the sampling of the phase relationship between the timing signal and the start of the frame pulse. A narrow bandwidth filter over the long term filters out virtually all of the phase error due to this poisson like distribution arising from the granularity assuming the PRS signal is highly stable; i.e., maintaining an accuracy in one part of 10^{13} over the course of a day. Thus, the use of such narrow bandwidth phase lock loops results in a much more tightly controlled synchronization once the phase lock loop has stabilized.

In particular, with a line clock at about a period of twenty nanoseconds, the best phase synchronization that could be attained would be on the order of twenty nanoseconds. However, by employing a one hertz bandwidth phase lock loop the phase error over the long term can be reduced to about one percent of this granularity or about the order of 0.2 nanoseconds. This phase lock loop can also be used for generating the 1.544 MHz timing reference signal required by the BITS clock at the node using a standard frequency multiplier configuration.

Further, to achieve phase lock during start up or after various transient conditions, it is preferable that

the bandwidth of the filter be adaptive as is readily possible with digital filters. During start up or after various transient conditions, the bandwidth of the loop is opened up, permitting faster acquisition of phase lock.

5 Upon detection of errors in either the CRC or upon detection of the predetermined bit pattern in any of the bits indicated with an X in Table 1 above indicating an error condition, the receiving node can go into a holdover node. Also, for such holdover conditions, the regenerated value can be ignored by the phase lock loop and the system can resort to the predicted values that may be generated by knowing the frequency of the frame rate and the timing reference signal. Alternatively, with such phase lock loops, the loop can be held at a nominal frequency until 10 the cause of the holdover condition is alleviated.

15 Also, the BITS clock can also be used for providing the timing signal temporarily when there is an error condition in the encoded coarse offset information, or the edge information, as shown in FIGURE 11. If an error is detected by the receiving office in the CRC, the edge bits, or a sudden change in the coarse offset value from a predicted value shows a loss of synchronization at the 20 transmitting office, the office generates an error signal

252. The output of the decoder 126 is provided to one input of a multiplexer 254. The other input is provided by dividing down the BITS clock 108 by eight hundred with divider 256 where the output of the divider is synchronized to valid rising edges of the regenerated signal according to well known techniques. The output of the divider 256 is coupled to the other input of the multiplexer 254 to provide a temporary backup version of the regenerated timing signal. Therefore, whenever the office detects an error condition, the error signals 252 can select the temporary back up signal to provide the regenerated timing signal 114.

For propagation of synchronization throughout the network, each node not serving as a master clock source can both receive and regenerate the timing reference signal and also generate a timing reference signal and transmit the difference between that generated timing reference signal and the frame. Since each node in the network receives and regenerates the same synchronization information, the network architecture is essentially flat. Further, timing loops are eliminated due to the usage of such a flat architecture.

Although a particular embodiment of the invention is

disclosed, alternatives would be readily apparent to those of skill in the field. Different frequencies for signals are, of course, appropriate for different networks such as OC-N or SDH where line clock frequencies are integer multiples of 51.84 MHz or 155 MHz, respectively. In fact, 5 a 19.44 MHz clock, which is readily available in many implementations, may also be used, instead of the actual line clock, to measure the timing difference. Also, different protocols can be used for encoding and 10 transmitting the timing difference signal. Instead of using counters to generate the timing difference various types of analog and digital phase detectors may be used. Alternatively, the regenerated timing signal could also be obtained through the use of a high precision numerically 15 controlled oscillator controlled by a microprocessor using the coarse offset information to generate the timing reference signal at the output of the oscillator. In addition, while the disclosed embodiments use the start of the frame as a reference for generating the timing difference, other specific times in the frame may also be 20 used for generating the timing difference with the local timing reference signal.

Further, instead of using the PRS as an original

source for the synchronization signal to be distributed, other sources may be used such as the disciplined time scale generator disclosed in U.S. Patent Application No. 08/278,423 to Zampetti, pages 9-26 of which are incorporated herein by reference. By equipping occasional offices in the chain with such timescale generators that are disciplined to a universal time scale such as GPS or LORAN, a highly synchronous network is established without requiring the expense of numerous PRS clocks or disciplined time scale generators at each office. Resort to the scope of the invention should be through the claims.

We claim:

1. A method of passing synchronization through a network comprised of a plurality of nodes communicating with each other at a predetermined frame rate, the nodes 5 communicating with each other through frames having predefined starts and with a line clock, the communication occurring by transmitting the frame and the line clock between nodes, the method comprising:

determining the timing difference between an event in 10 one timing signal based upon another timing signal occurring during the time for the transmission of a first frame;

encoding that timing difference in data packets transmitted during a plurality of subsequent frames; and 15 encoding in the subsequent frames information indicative during which prior frame the event occurred.

2. The method of claim 1, wherein the method further includes encoding the timing difference 20 with a number of bits greater than the number of bits necessary to encode the timing difference, whereby extra bits are provided.

3. The method of claim 2, wherein at least some of the extra bits are used for transmitting the occurrence of an error condition.

4. The method of claim 3, wherein each of the timing signals have a phase associated with the signal and at least some of the extra bits indicate that a phase slippage greater than a predetermined threshold has occurred.

5. An apparatus for encoding of phase information related to two signals in a network using frame messaging between nodes related to an event occurring in less than all of the frames, a first of the signals being a clock signal and the second of the signals being related to frame timing, the apparatus comprising:

means for determining the timing difference between the clock signal and the frame timing for at least one frame;

means for encoding the timing difference in a plurality of bits to be transmitted over a plurality of subsequent frames; and

means for indicating in an additional plurality of bits during which frame the event occurred.

6. The apparatus of claim 5, wherein the apparatus further comprises:

means for determining if the timing difference exceeds a predetermined threshold; and

5 means for encoding in the plurality of bits information indicative of the timing difference exceeding the predetermined threshold.

7. The apparatus of claim 5, wherein the event occurs at a rate of less than or equal to once 10 every predetermined number of frames, the means for encoding further including:

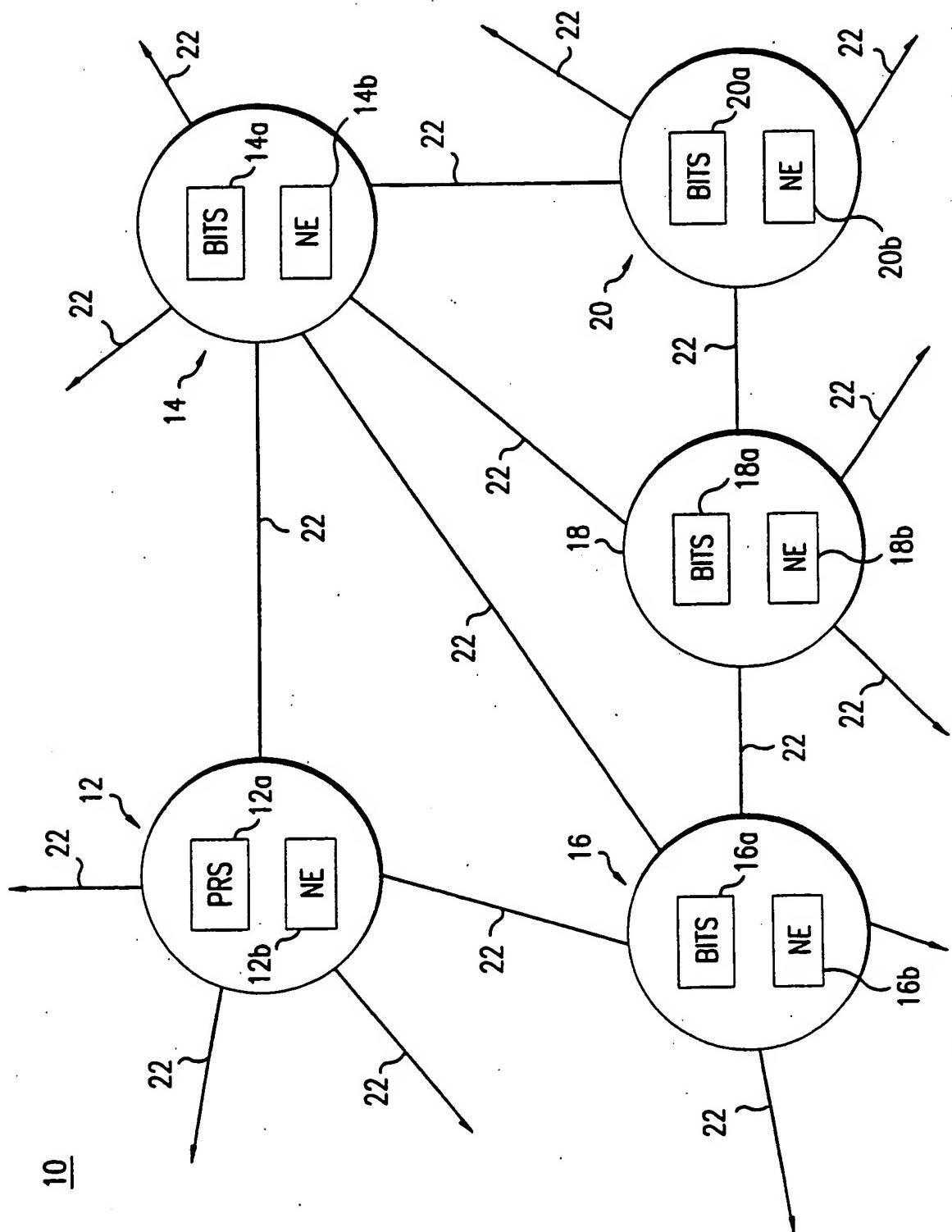
means for representing the timing difference in a plurality of bits;

15 means for dividing the representation of the timing difference into a plurality of packets, one packet to be transmitted per frame;

means for encoding in which prior frame the event occurred; and

20 means for transmitting over an odd plurality of frames the encoded information indicating in which prior frame the event occurred.

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FIG. 1

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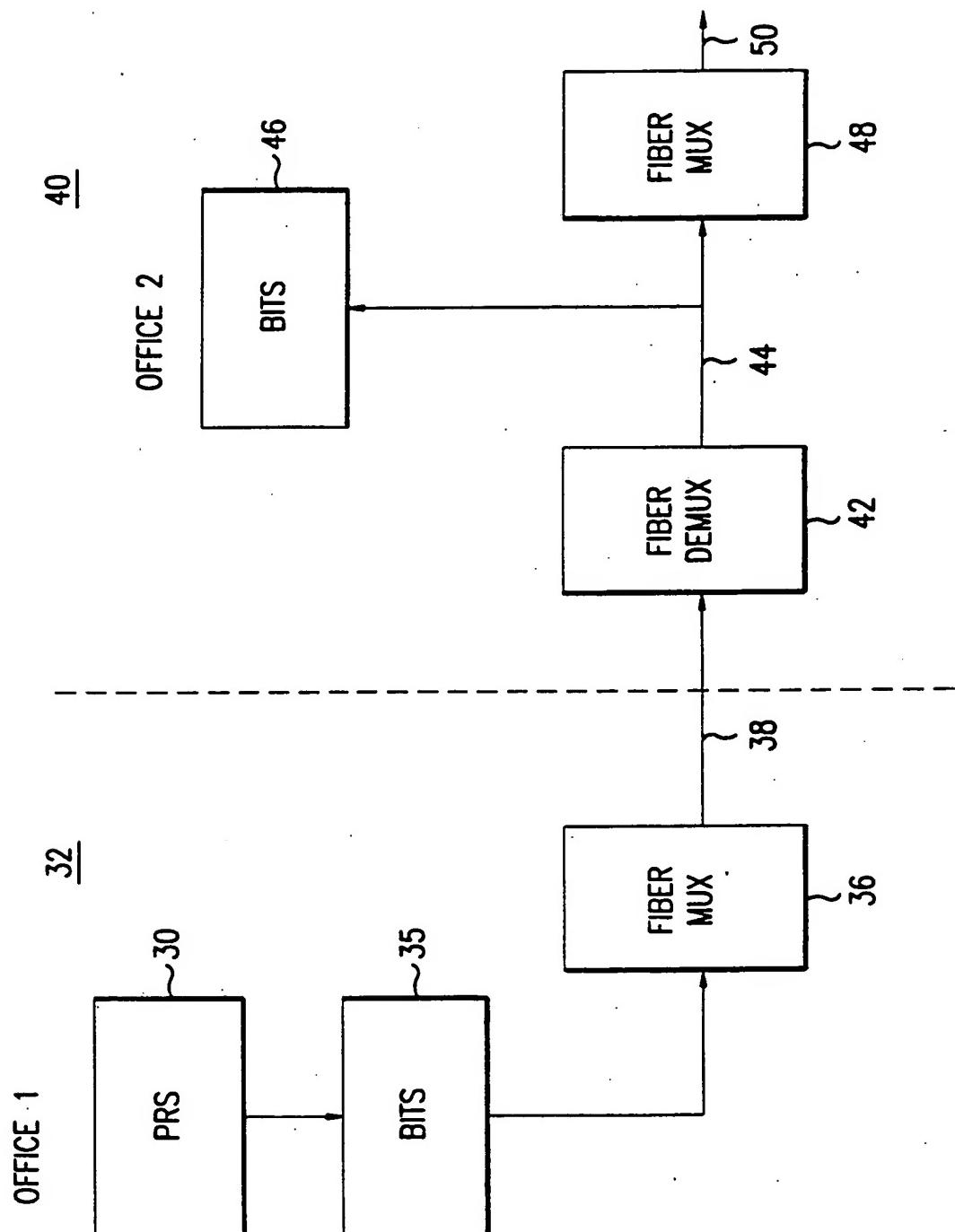
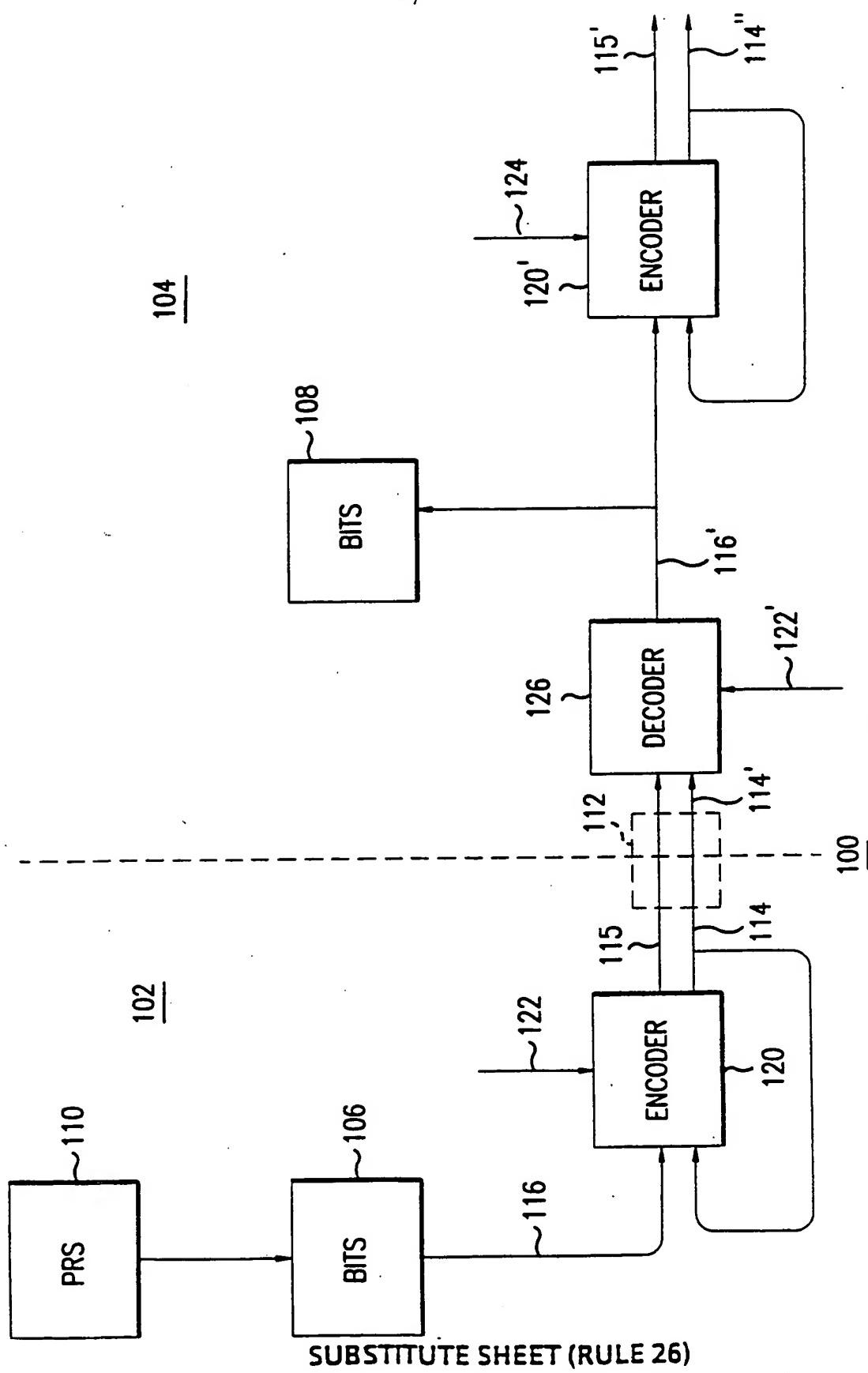


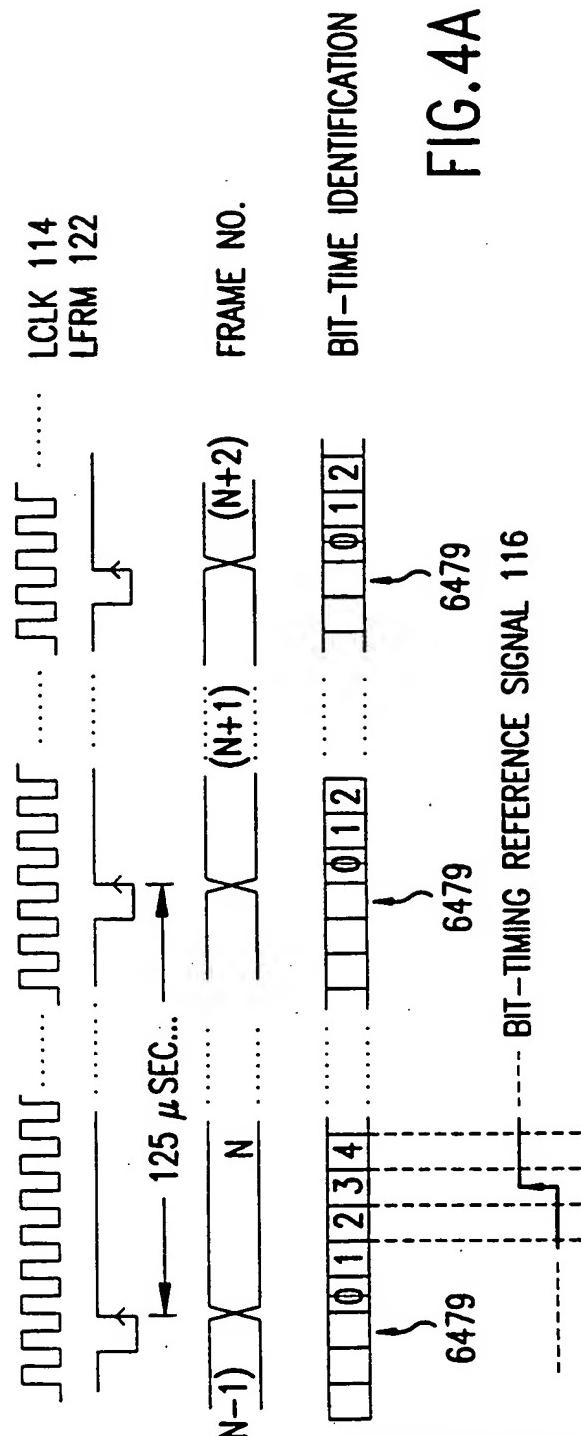
FIG.2

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FIG. 4A

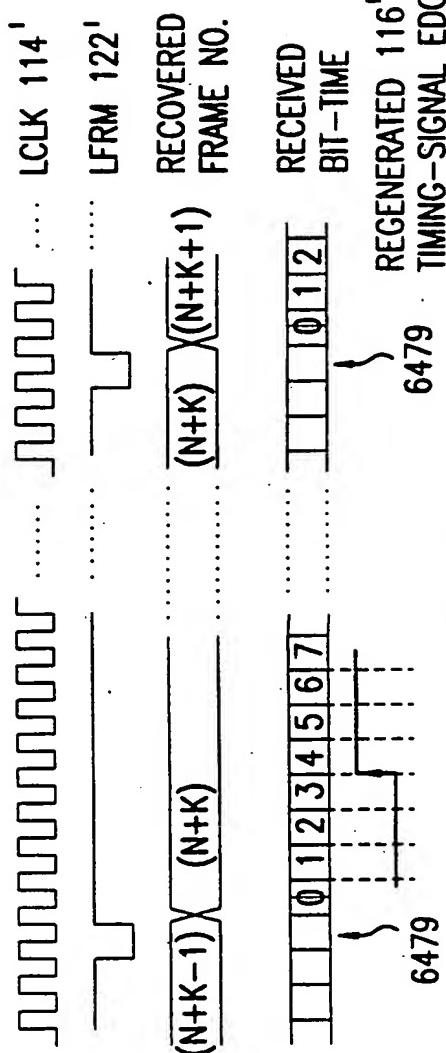


FIG. 4B

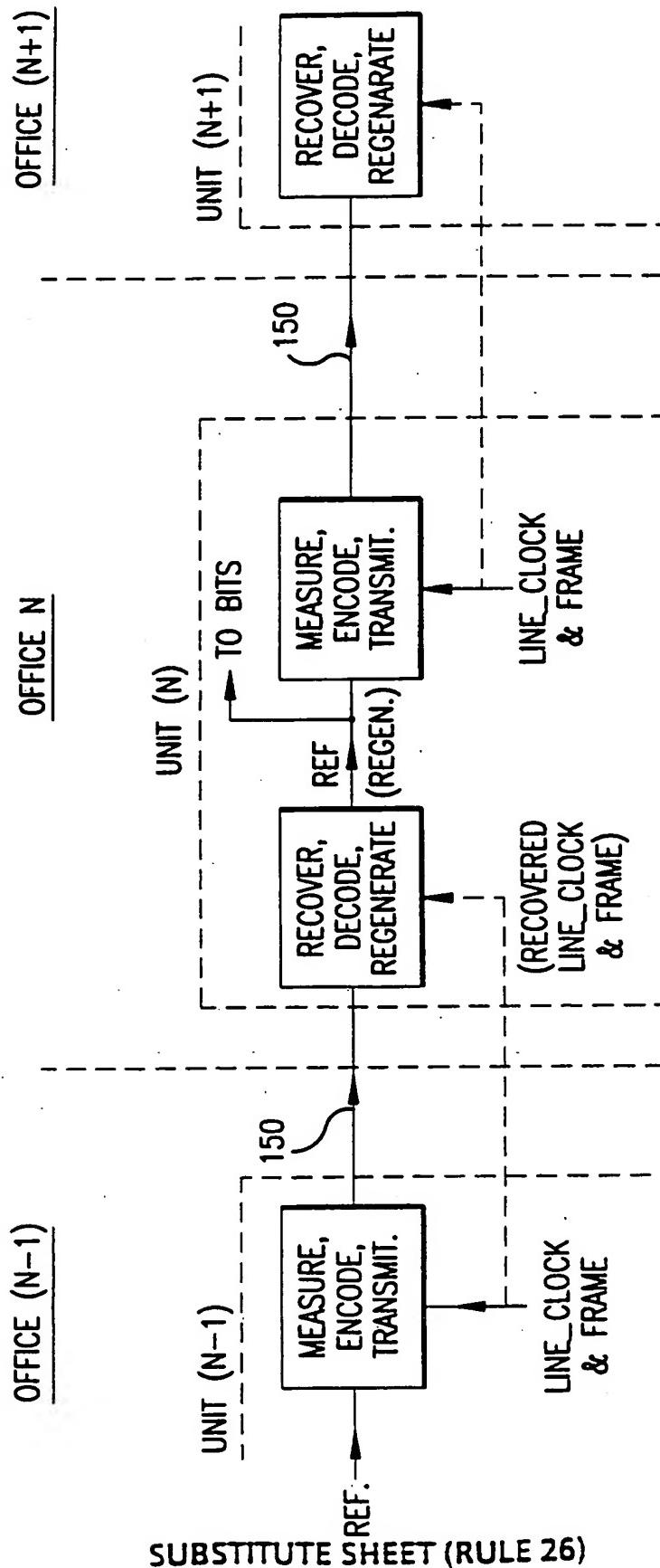
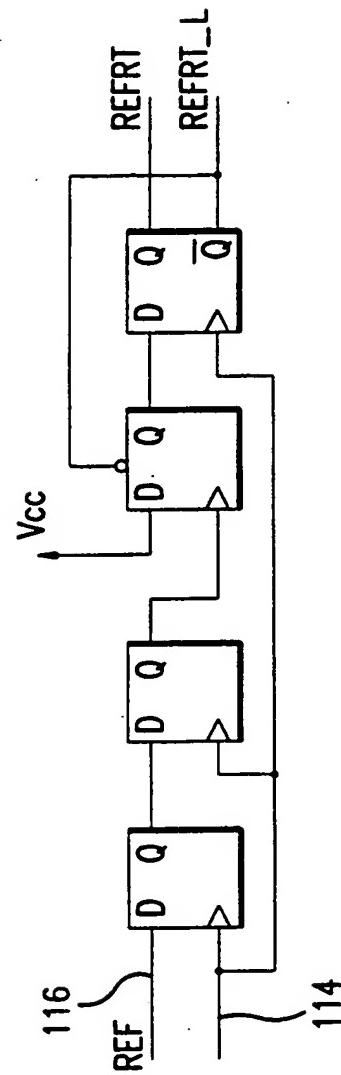
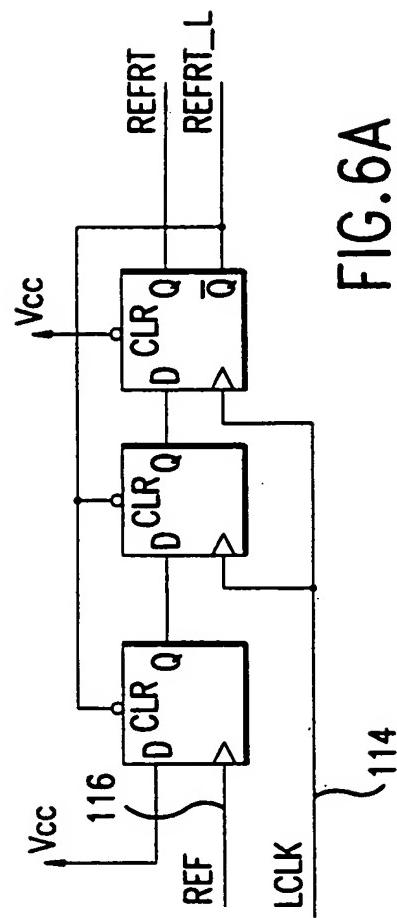


FIG.5

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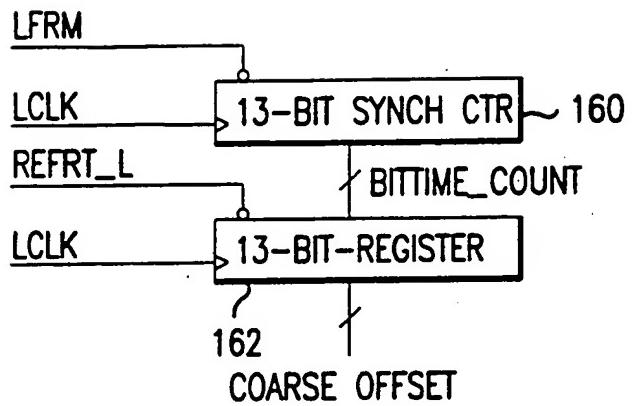


FIG.7A

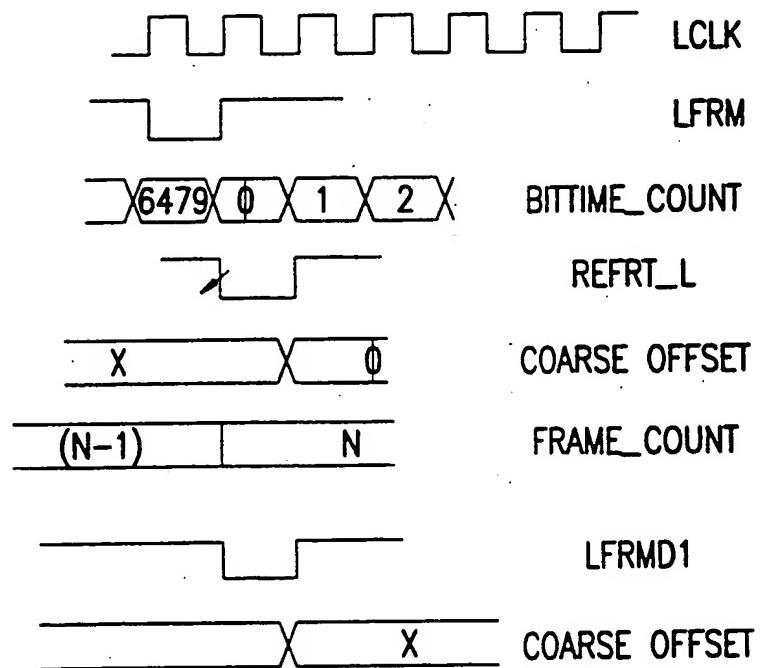


FIG.7B

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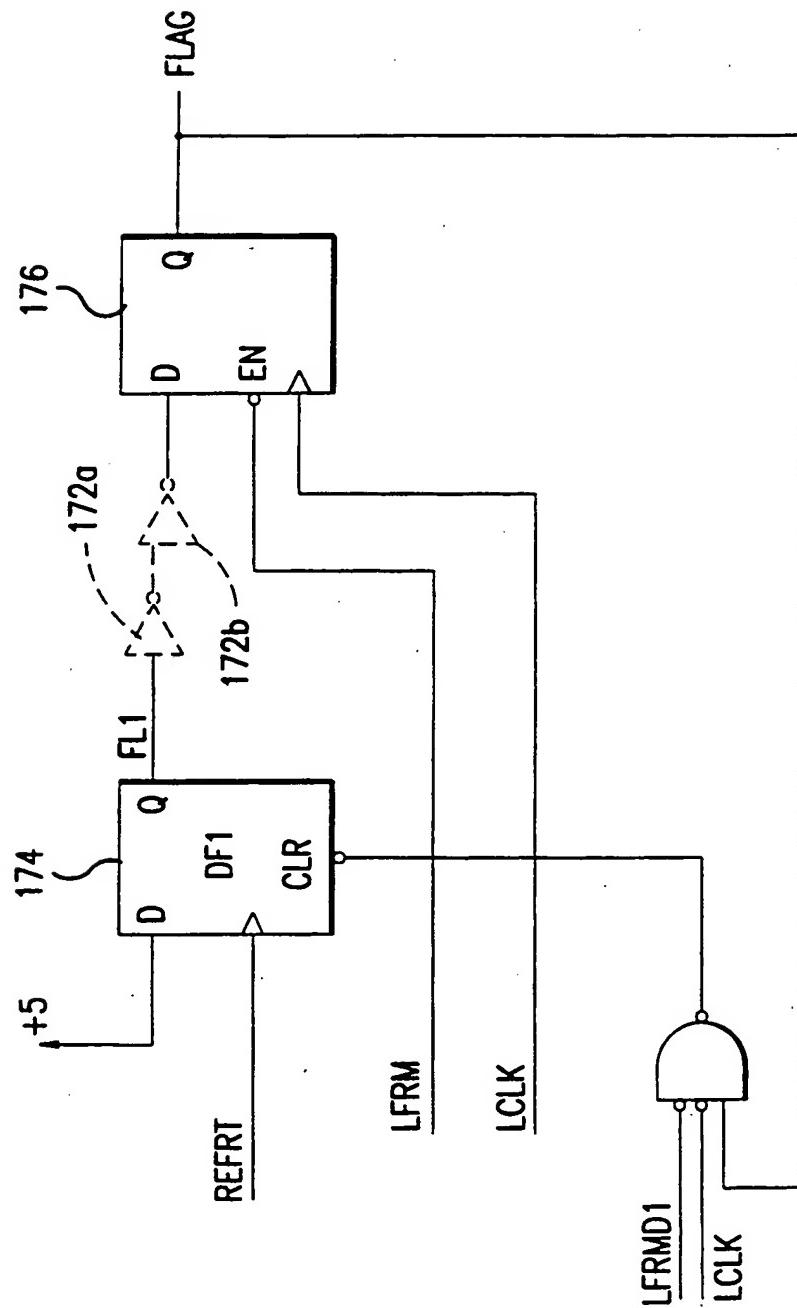


FIG.8

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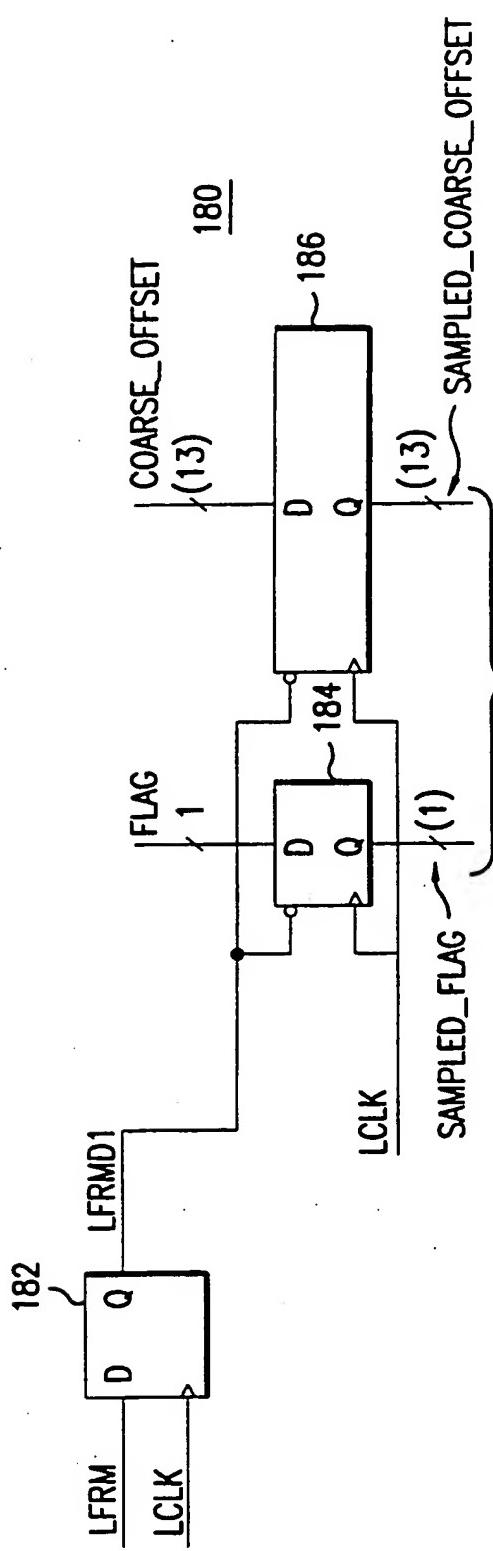


FIG. 9A FLAG_OFFSET

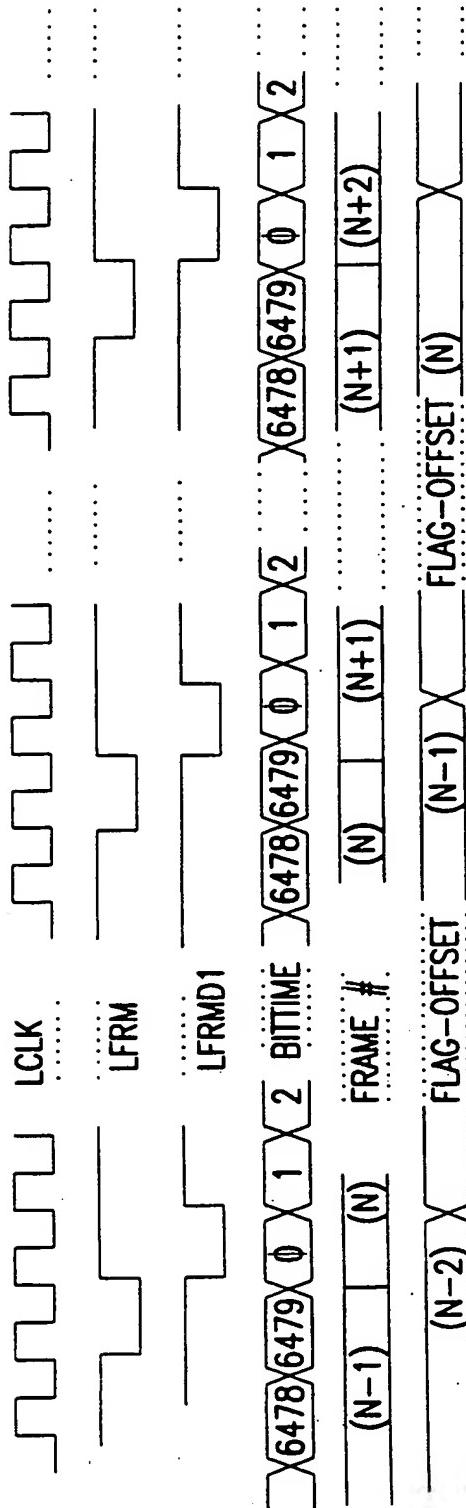


FIG. 9B

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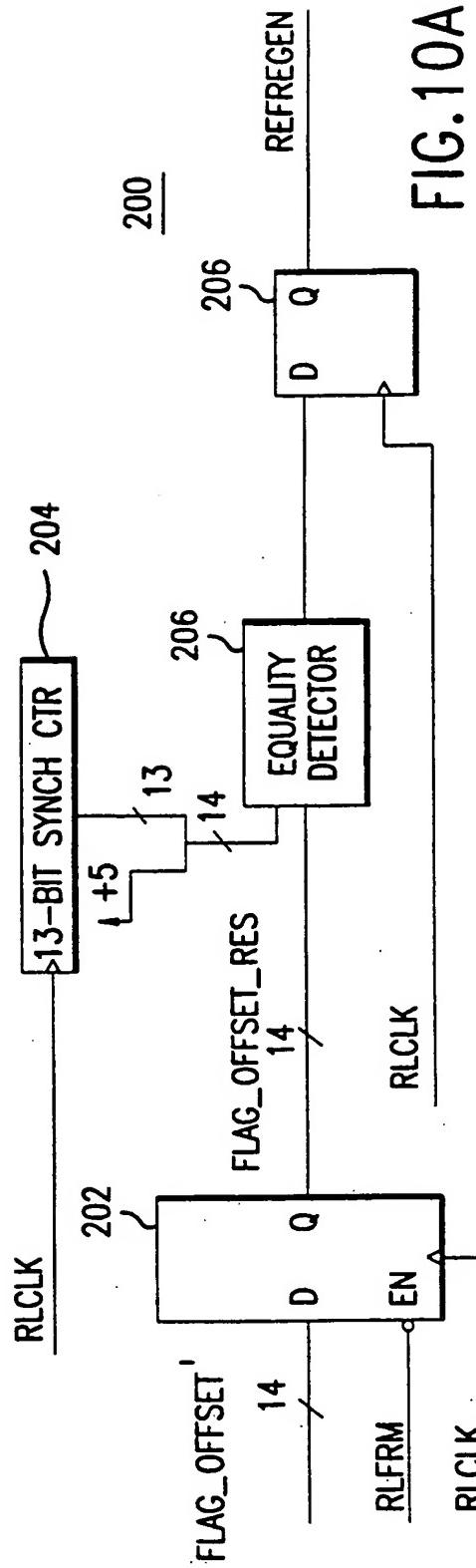


FIG. 10A

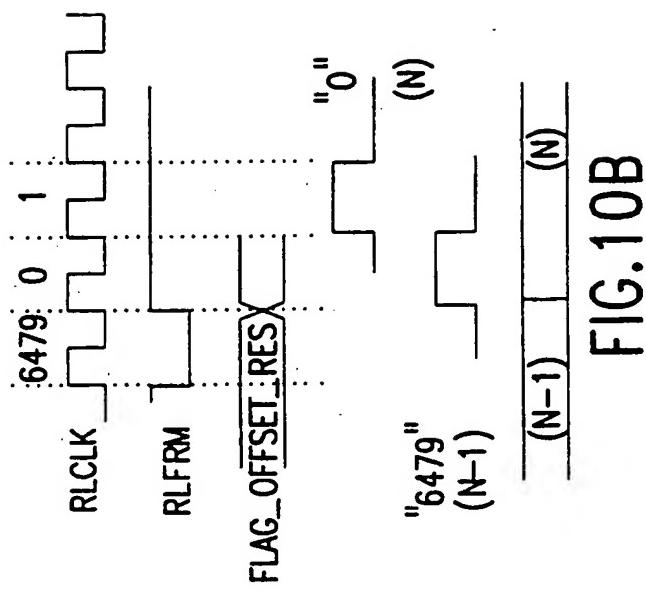


FIG. 10B

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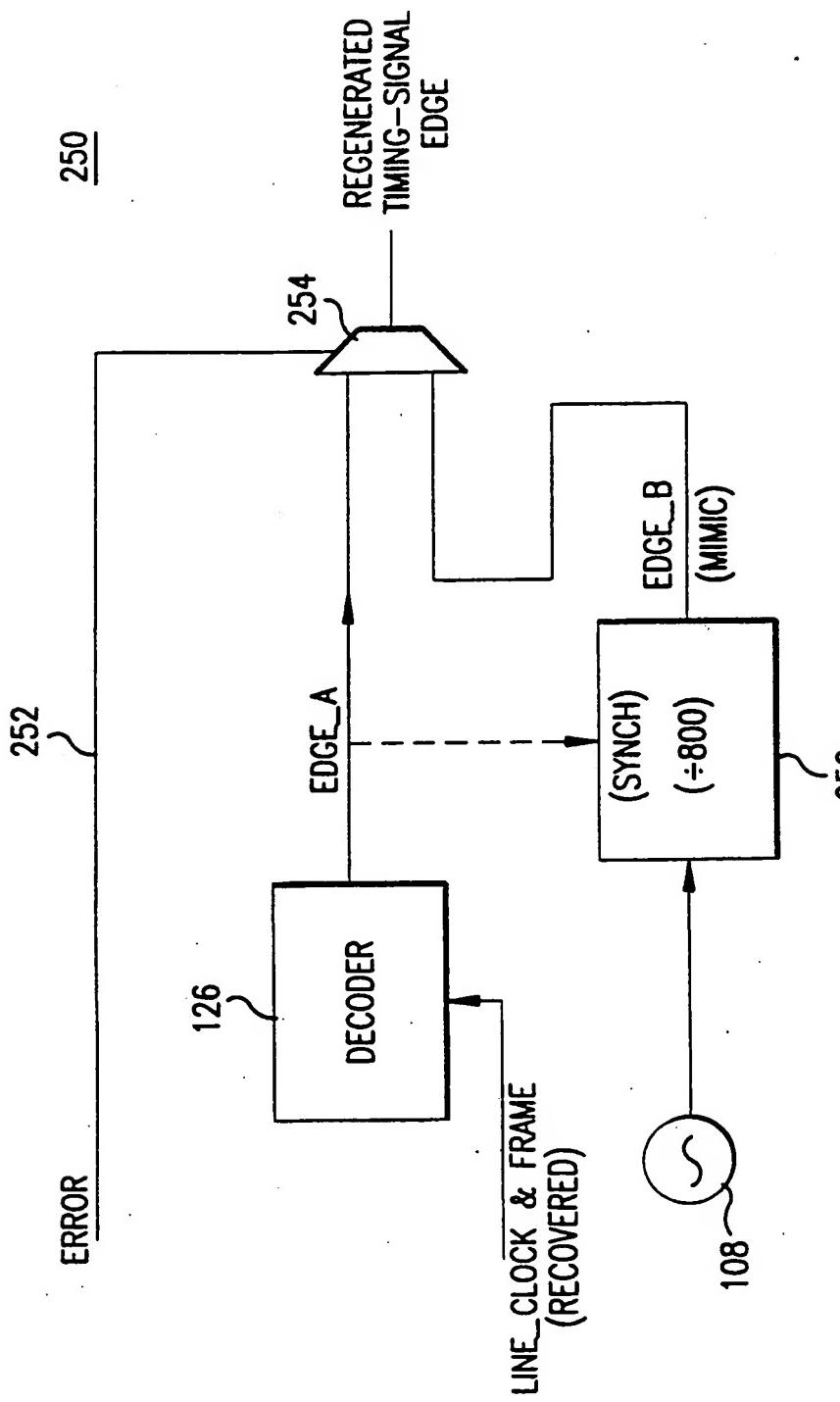


FIG. 11

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INTERNATIONAL SEARCH REPORT

Internal Application No
PCT/US 96/07909

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04J3/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,5 241 543 (AMADA EIICHI ET AL) 31 August 1993 see column 4, line 19 - line 53 see column 5, line 1 - line 23 see column 7, line 31 - line 41 see column 8, line 22 - line 51 see column 10, line 66 - column 12, line 11 see figures 3-10 ---	1-3
A	---	4-7 -/-

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

* Special categories of cited documents :

- *'A' document defining the general state of the art which is not considered to be of particular relevance
- *'E' earlier document but published on or after the international filing date
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Date of the actual completion of the international search

27 August 1996

Date of mailing of the international search report

13.09.96

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax (+31-70) 340-3016

Authorized officer

Pieper, T

INTERNATIONAL SEARCH REPORT

Intern'l Application No
PCT/US 96/07909

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>COMMUNICATION FOR GLOBAL USERS, INCLUDING A COMMUNICATIONS THEORY MINI CONFERENCE ORLANDO, DEC. 6 - 9, 1992, vol. 1 - 2 - 03, 6 December 1992, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 814-820, XP000357678 LAU R C ET AL: "SYNCHRONOUS TECHNIQUES FOR TIMING RECOVERY IN BISDN" see page 815, right-hand column, paragraph 2 - page 816, left-hand column, line 1 see page 816, right-hand column, paragraph 2 - page 817, right-hand column, paragraph 1; figures 3-6</p> <p>---</p>	5,7
A	<p>EP,A,0 460 835 (PLESSEY TELECOMM) 11 December 1991 see column 4, line 38 - line 41 see column 6, line 22 - line 38 see column 7, line 14 - line 27 see figures 1-3</p> <p>---</p>	1,5
A	<p>US,A,4 489 421 (BURGER ERICH) 18 December 1984 see column 1, line 54 - column 2, line 43 see column 3, line 19 - line 55 see column 4, line 34 - column 5, line 9 see figures 1,2</p> <p>-----</p>	1,5,7

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 96/07909

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		JP-C-	1599928	31-01-91
		JP-B-	2025576	04-06-90
		JP-A-	58131850	05-08-83
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